Unit-IV:Amplifiers
PHY-HC-4036
Prepared by
Dr. Ananya Phukan

January 20, 2024

1 Transistor Biasing & Stabilization Circuits

A transistor can be used as an amplifier by forward biasing the emitter base junction and reverse biasing the collector base junction. The purpose of this dc biasing is to make the transistor work in the active region and to get a certain dc collector current I_C at a certain dc collector voltage (V_{CE}). These values of I_C and V_{CE} are expressed by operating point or quiescent point (Q - point). The position of the Q-point on the dc load line determines the maximum signal that we can get from the circuit.
Transistor biasing means the establishment of the Q-point in the desired position of the load line by connecting the transistor to external voltage sources via appropriate circuits. The circuits which provide transistor biasing are called biasing circuit. The Q-point should be stable with respect to temperature fluctuations and replacement of the transistor by an equivalent transistor. The process of making operating point independent of temperature changes or change of transistor parameters is known as stabilization.

1.1 Need for stabilisation

The operating point or Q-point can change due to the instability of the collector current I_C. The sources for the instability of the collector current are:

i. The reverse saturation current I_{C0} which doubles for every $10°C$ rise of temperature.

ii. The base-emitter voltage V_{BE} that falls at the rate of $2.5mV/°C$ for both Ge and Si transistors.

iii. β which rises with temperature. The value of β can also change when one transistor is replaced by another.

1.2 Stability Factor

The degree of success achieved in stabilizing collector current with respect to the variation in the reverse saturation current is expressed in terms of stability factor (S). it is defined as the rate of change of collector current (I_C) with respect to change of reverse saturation current I_{C0} when I_B is constant, i.e.,

$$S = \frac{dI_C}{dI_{C0}}$$

The lower the stability factor, the better the stability of the Q-point. The lowest value of S is unity.

1.3 Thermal runaway

An increase of temperature enhances I_{C0} and hence the collector current I_C. The increased collector current heats the collector junction, which in turn, increases I_{C0} further. The process is cumulative in nature, causing the junction temperature to exceed its rated value. The transistor can be damaged. This phenomenon is referred to as thermal runaway. To avoid thermal runaway, some form of stabilizing circuit is therefore necessary.

2 Methods of Transistor biasing

2.1 Fixed Bias or Base bias method

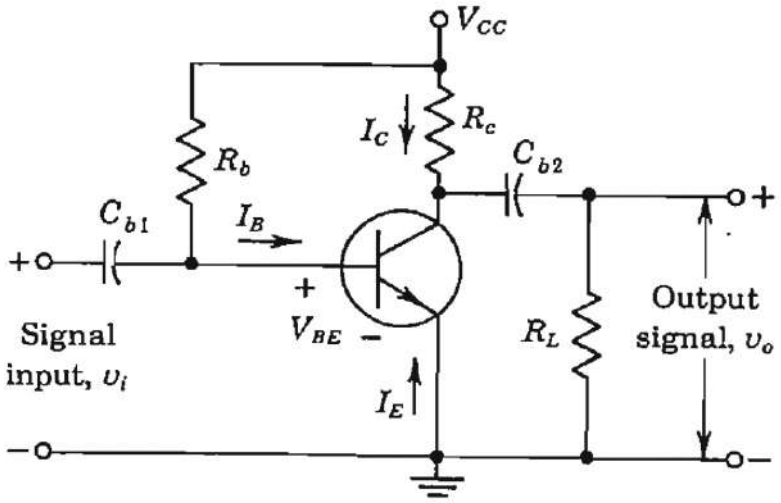

Figure 1: Fix bias circuit for CE n-p-n transistor

The fixed bias or base bias arrangement for an $n-p-n$ transistor operating in the CE-mode is shown in Fig. 1. The voltage source V_{CC} makes the emitter-base junction forward-biased and the collector-base junction reverse-biased. It also supplies the quiescent (i.e. zero signal) base and collector currents. A high resistance R_b is connected between the base and V_{CC} which determines the flow of quiescent base current (I_B) and collector current (I_C). A voltage drop V_{BE} develops between the base and the emitter.
Applying Kirchoff's voltage law in the base emitter closed loop:

$$V_{CC} = I_B R_b + V_{BE}$$
$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_b}$$

Since, V_{BE} is very small (≈ 0.75 for Si), so $V_{CC} >> V_{BE}$
Therefore,

$$I_B = \frac{V_{CC}}{R_b} \tag{1}$$

Since, V_{CC} is fixed and by choosing a value of R_b, the base current I_B can be made constant. Hence this circuit is called **fixed bias circuit**.

Stability Factor

The quiescent (Q) point is usually selected in the active region of the characteristics. The collector current is then given by,

$$I_C = \beta I_B + (\beta + 1) I_{C0}$$

Differentiating w.r.t I_C

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{C0}}{dI_C}$$

$$\Rightarrow 1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left(\because S = \frac{dI_C}{dI_{C0}} \right)$$

In fixed bias method, I_B is independent of I_C, so $\dfrac{dI_B}{dI_C} = 0$

$$\therefore 1 = \frac{\beta + 1}{S}$$

$$\Rightarrow S = \beta + 1 \tag{2}$$

Since, the current gain (β) has high value, so the stability factor of fixed bias is very high and therefore it has poor thermal stability.

2.2 Emitter bias or Voltage Divider bias method

The emitter bias or voltage-divider bias circuit as shown in Fig.2 is commonly used to establish a stable operating point. The forward bias to the emitter-base junction and the reverse bias of the collector-base junction are provided by the supply voltage V_{CC} through the resistance R_1, R_2, R_E and R_L. As R_1 and R_2 serve as the voltage-divider, the arrangement is referred to as the voltage divider bias.The current in the resistance R_E causes a voltage drop which is in the direction to reverse-bias the emitter junction. Since this junction must be forward-biased, the base voltage is obtained from the supply through the $R_1 R_2$ network. The physical reason for an improvement in stability with this circuit is as follows: If I_C tends to increase, say, because I_{C0} has risen as a result of an elevated temperature, the current in R_E increases. As a consequence of the increase in voltage drop across R_E, the base current is decreased. Hence I_C will increase less than it would have, had there been no self-biasing resistor R_E.

Determination of Q-point

If the circuit to the left between the base B and ground G terminals in Fig.3 is replaced by its Thevenin equivalent source, we obtain voltage V_{TH} and internal resistance R_{TH}

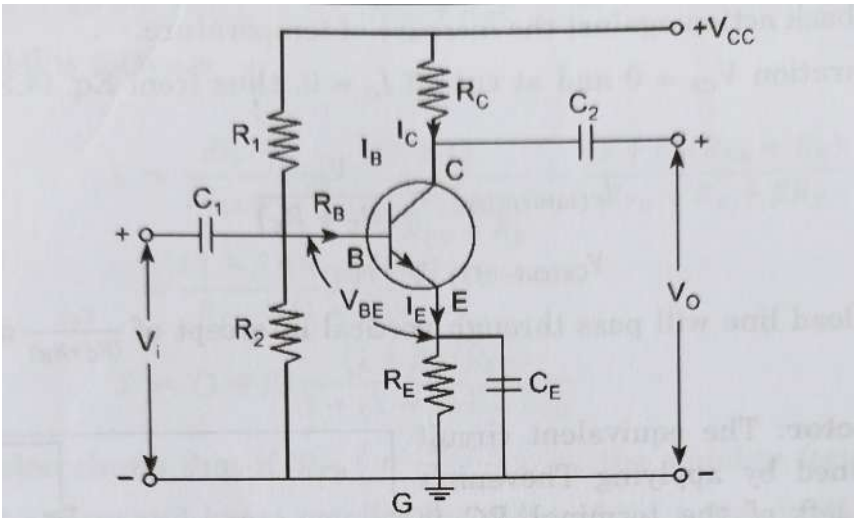

Figure 2: Voltage divider bias in common-emitter $n-p-n$ transistor

$$V_{TH} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{3}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{4}$$

Applying Kirchoff's voltage law around the base circuit, we get

$$I_B R_{TH} + V_{BE} + (I_B + I_C) R_E = V_{TH} \tag{5}$$

$$I_B = \frac{V_{TH} - V_{BE} - I_C R_E}{R_{TH} + R_E} \tag{6}$$

Now applying Kirchoff's voltage law around the collector circuit, we get

$$I_C R_L + V_{CE} + (I_B + I_C) R_E = V_{CC} \tag{7}$$

As $I_C >> I_B$, we can neglect $I_B R_E$ compared to $I_C R_E$

$$\therefore V_{CE} = -(R_L + R_E) I_C + V_{CC} \tag{8}$$

or

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \tag{9}$$

Eq.8 shows that the relationship between I_C and V_{CE} is a straight line of slope $-1/(R_L+R_E)$and an intercept of V_{CC} on the V_{CE} axis. This straight line is the dc load line drawn on the collector characteristics. To draw the bias curve, I_C from Eq. 5 is substituted into Eq.7. A relationship between I_B and V_{CE} is thus achieved. The locus of the points V_{CE} and I_B plotted on the output

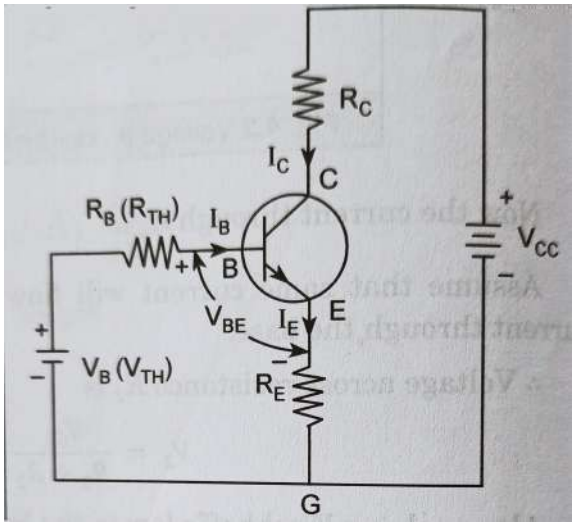

Figure 3: Thevinin Equivalent Circuit

characteristics is termed the bias curve as shown in Fig.4. The intersection of the dc load line and the bias curve gives the quiescent point Q.

Stability Factor

The Q-point can be found by noting that in the active region the collector current is given by;

$$I_C = \beta I_B + (1+\beta) I_{C0} \tag{10}$$

Putting I_B from Eq.6 in above Eq. 10, we get

$$I_C = \beta \left(\frac{V_{TH} - V_{BE} - I_C R_E}{R_{TH} + R_E} \right) + (1+\beta) I_{C0}$$

$$I_C \left(1 + \frac{\beta R_E}{R_{TH} + R_E} \right) = \frac{\beta V_{TH}}{R_{TH} + R_E} - \frac{\beta V_{BE}}{R_{TH} + R_E} + (1+\beta) I_{C0}$$

Differentiating both sides w.e.t. I_{C0}

$$\frac{dI_C}{dI_{C0}} \left(1 + \frac{\beta R_E}{R_{TH} + R_E} \right) = 1 + \beta$$

$$\frac{dI_C}{dI_{C0}} = \frac{1+\beta}{1 + \dfrac{\beta R_E}{R_{TH} + R_E}}$$

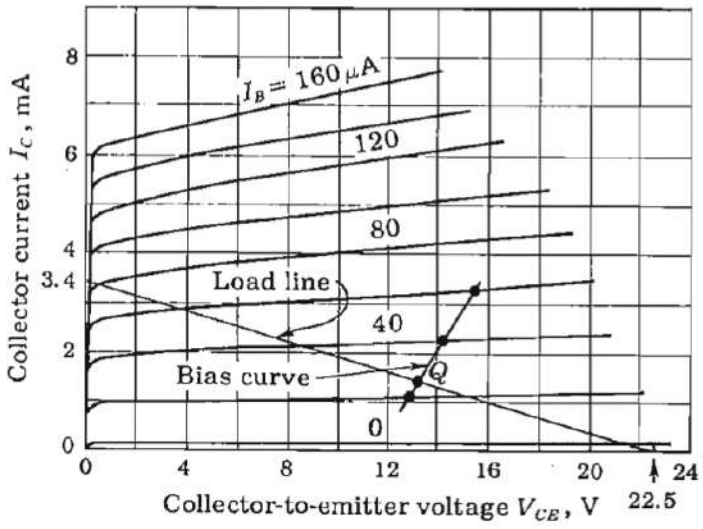

Figure 4: Intersection of the load line and the bias curve determines the Q point

$$S = \frac{dI_C}{dI_{C0}} = (1+\beta)\frac{R_{TH}+R_E}{R_{TH}+R_E+\beta R_E}$$

$$S = (1+\beta)\frac{1+\dfrac{R_{TH}}{R_E}}{1+\beta+\dfrac{R_{TH}}{R_E}}$$

This expression shows that if $R_{TH}\left(=\dfrac{R_1R_2}{R_1+R_2}\right) < R_E$, the stability factor of the voltage divider bias will be low and hence smaller the value of R_{TH} better is the stabilization.
If $R_T << R_E$, $S = 1$, which indicates maximum stability.

3 Transistor as 2-port Network

After the establishment of the Q-point, ac signals (ie, ac current or voltage) are applied to a pair of input terminals (or input port) of the transistor amplifier. The amplified signal appears at a pair of output terminals (called output port) of the amplifier. For a small amplitude of the input signal, the operation of the transistor is confined to the linear region of the characteristic curve of the transistor. This linear performance of the amplifier can be studied analytically by considering the transistor in any one of its three modes (CB, CE or CC). The terminal behavior of such a two-port device is usually determined by four variables: two signal currents i_1 and i_2 and two signal voltages v_1 and v_2. For transistors, the input current i_1 and output voltage v_2 are independent variables, and the input voltage v_1 and the output current i_2 as the dependent variables. The dependent variables are related to the independent variables by

$$v_1 = h_{11} i_1 + h_{12} v_2 \tag{11}$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \tag{12}$$

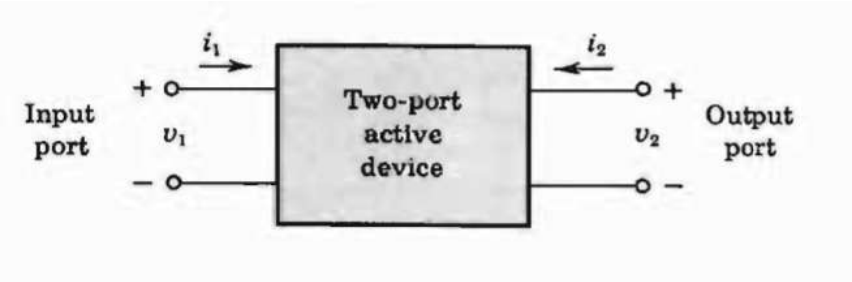

Figure 5: A two-port network

The quantities h_{11}, h_{12}, h_{21} and h_{22} are called the **h** or ***hybrid parameters*** because they are not all alike dimensionally.
Then, from Eq. 11 and 12, the **h** parameters are defines as follows:

$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2=0} = \textit{input resistance} \text{ with output short-circuited for ac}$$

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1=0} = \textit{reverse voltage amplification factor} \text{ with the input port open-circuited to ac}$$

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0} = \textit{short-circuit current gain}$$

$$h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1=0} = \textit{output admittance or conductance} \text{ with the input open-circuited}$$

Notation for h parameters are:

$i = 11 =$ input
$o = 22 =$ output
$f = 21 =$ forward transfer
$r = 12 =$ reverse transfer

A second transcript (b, e or c) is included to designate the circuit configuration. For example

$h_{ib} = h_{11b} =$ input resistance in common-base configuration
$h_{fe} = h_{21e} =$ short-circuit forward current gain in common-emitter circuit

The hybrid parameters have the following advantages:

i. At audio frequencies, the h-parameters are real numbers because of the absence of reactive elements in the two-port device.

ii. h-parameter can be readily measured. They can also be determined from the transistor static characteristic curves.

iii. The h-parameters are convenient to use in circuit analysis and design.

iv. They offer simple mathematical expressions for the performance quantities like current, voltage and power gains , input and output impedences etc.

4 h-parameter Equivalent Circuit

The four h parameters which are real numbers are used to construct an equivalent circuit of the two-port device. This equivalent circuit is called the ***hybrid model*** or ***h-equivalent circuit*** as shown in Fig. 6.
We can verify that application of Kirchoff's voltage and current laws for the input and the output circuits of Fig. 6 satisfies Eq. 11 and 12. Applying the notation for h-parameters, Eq. 11 and 12 is written as:

$$v_1 = h_i i_1 + h_r v_2 \tag{13}$$

$$i_2 = h_f i_1 + h_o v_2 \tag{14}$$

Since the voltages and currents in Fig. 6 are the signal or the ac values, the equivalent circuit represented in the figure is the ac equivalent circuit.

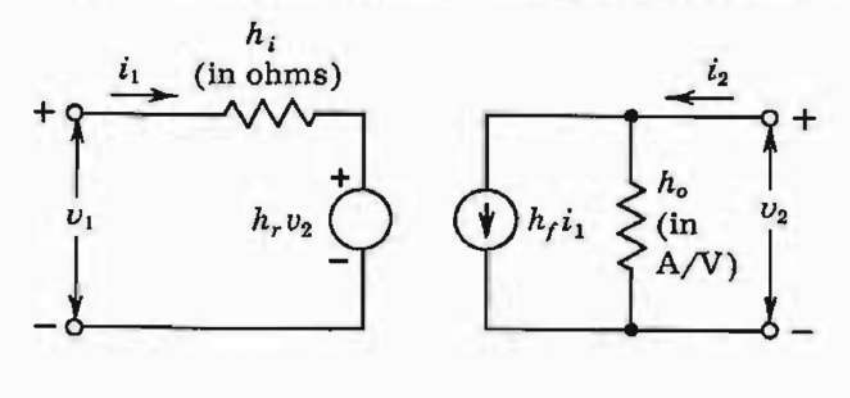

Figure 6: h-equivalent circuit of a two-port network. The parameters h_r and h_f are dimensionless.

NOTE:

1. From Eq. 13,

- The first component is the voltage drop ($h_i i_1$) across resistance h_i due to the flow of input current i_1 across it.
- The second component is proportional to output voltage v_2. It is represented by a constant voltage generator $h_r v_2$.

Thus, the input circuit appears as a resistance h_i in series with a voltage generator $h_r v_2$.

2. From Eq. 14,

- The first component is the voltage drop ($h_f i_1$) is proportional to i_1. It is represented by a constant current generator $h_f i_1$.
- The second component is the current portion flowing through the admittance h_o. It provides low reactance path. So it behaves as a shunt resistance parallel to $h_f i_1$.

Thus, the outut circuit appears as an admittance h_o parallel to the current generator $h_f i_1$.

4.1 Determination of h-parameters from transistor characteristics

The basic assumption in arriving at a transistor equivalent circuit is that the variations about the quiescent (Q) point is assumed to be small, so that the transistor parameters can be considered constant over the signal excursion.
To see how we can derive the h-parameters of a transistor, let us consider the common-emitter (CE) configuration. The instantaneous total values of the input and the output currents are i_B and i_C respectively. The instantaneous total values of the input and the output voltages are $v_{BE} = v_B$ and $v_{CE} = v_C$ respectively. Since v_B is some function f_1 of i_B and v_C and since i_C is another function f_2 of i_B and v_C, we can write

$$v_B = f_1(i_B, v_C) \tag{15}$$

$$i_C = f_2(i_B, v_C) \tag{16}$$

Expanding Eqs 19 and 20 in a Taylor's series about the quiescent values I_B and V_C, and neglecting higher-order terms, we get

$$\Delta v_B = \left.\frac{\partial v_B}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial v_B}{\partial v_C}\right|_{I_B} \Delta v_C \tag{17}$$

and

$$\Delta i_C = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial i_C}{\partial v_C}\right|_{I_B} \Delta v_C \tag{18}$$

Here, the partial derivatives are taken, keeping the collector voltage or the base current constant, as denoted by the subscript attached to the derivatives.

The quantities Δv_B, Δv_C, Δi_B and Δi_C represent the small-signal base and collector voltages

and currents, which are the instantaneous values of the ac components v_b, v_c, i_b and i_c. Therefore Eqs. 17 and 18 can be written as

$$v_b = h_{ie} i_b + h_{re} v_c \tag{19}$$

and

$$i_c = h_{fe} i_b + h_{oe} v_c \tag{20}$$

where

$$h_{ie} = \left.\frac{\partial v_B}{\partial i_B}\right|_{V_C}, \qquad h_{re} = \left.\frac{\partial v_B}{\partial v_C}\right|_{I_B}$$

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C}, \qquad h_{oe} = \left.\frac{\partial i_C}{\partial v_C}\right|_{I_B}$$

The partial derivatives defining the h-parameters in the above equations can be obtained from the transistor characteristic curves.

5 Analysis of a single-stage CE amplifier using Hybrid Model

The simple circuit diagram of a single stage common emitter $n-p-n$ transistor amplifier is shown in Fig. 7. This amplifier is applicable only for small signal low frequency amplification.The input signal source V_S with internal resistance R_S that will be amplified is connected in the input. A load resistance R_L is connected to the output. The biasing voltages V_{BB} and V_{CC} and load resistance R_L are selected so as to fix the Q-point at the middle of the load line as well as the linear region of the output characteristics.

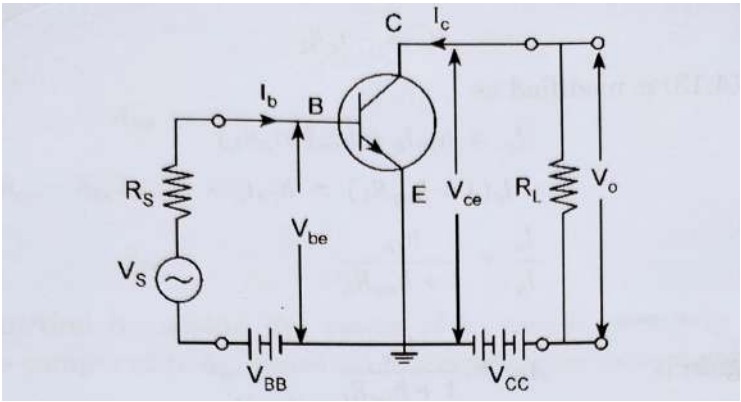

Figure 7: Common-emitter transistor circuit

The ac equivalent circuit using h-parameters of a CE transistor is shown in Fig.8. The equations for this equivalent circuit with h-parameters are:

$$V_i = h_{ie} I_b + h_{re} V_o \tag{21}$$

and

$$I_c = h_{fe} I_b + h_{oe} V_o \tag{22}$$

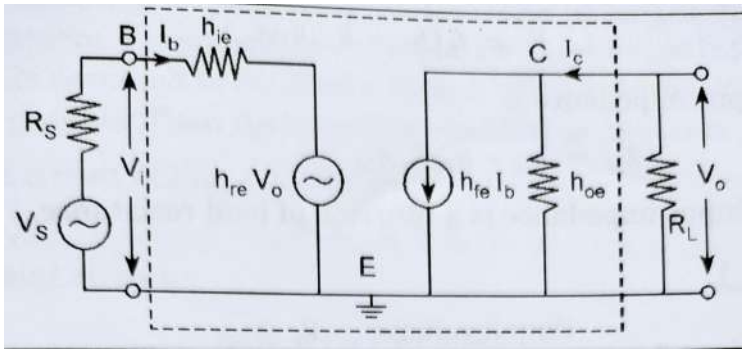

Figure 8: h-parameter equivalent circuit of a CE transistor

Using this h-parameter equivalent circuit, we can calculate current gain, voltage gain, input and output impedences and power gain of the common emitter transistor amplifier.

(a) Current Gain or Current Amplification (A_{ie})

Current Gain or Current Amplification (A_{ie}) is defined as the ratio of the output current to the input current. Thus current gain is

$$A_{ie} = \frac{I_o}{I_i} = \frac{I_c}{I_b}$$

The output voltage is the voltage across the load resistance, if the current through the load from positive terminal to the negative terminal is I_L, then

$$V_o = I_L R_L$$

But current I_C in the output circuit flows in opposite direction, thus

$$V_o = -I_c R_L$$

Thus Eq. 22 becomes,

$$\begin{aligned} I_c &= h_{fe} I_b + h_{oe}(-I_c R_L) \\ I_c(1 + h_{oe} R_L) &= h_{fe} I_b \\ \frac{I_c}{I_b} &= \frac{h_{fe}}{1 + h_{oe} R_L} \end{aligned}$$

Thus current gain is

$$A_{ie} = \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} R_L} \tag{23}$$

(b) Input Impedence (Z_{ie})

The input impedence (Z_{ie}) of the amplifier is the impedence we encounter looking into the input terminals B and E as shown in the equivalent circuit (Fig. 8) and is given by,

$$Z_{ie} = \frac{V_i}{I_i} = \frac{V_i}{I_b}$$

On substituting the value of $V_o = -I_c R_L$, Eq. 21 becomes

$$\begin{aligned} V_i &= h_{ie} I_b + h_{re} - I_c R_L \\ V_i &= I_b (h_{ie} - h_{re} R_L \frac{I_c}{I_b}) \\ V_i &= I_b (h_{ie} - h_{re} R_L A_{ie}) \end{aligned}$$

Therefore the input impedence is,

$$Z_{ie} = h_{ie} - h_{re} R_L A_{ie} \tag{24}$$

This shows that input impedence is a function of load resistance.

(c) Voltage Gain (A_{ve})

The voltage gain is

$$\begin{aligned} A_{ve} &= \frac{Output\ voltage}{Input\ voltage} = \frac{V_o}{V_i} \\ A_{ve} &= -\frac{I_c R_L}{V_i} = -\frac{I_c}{I_b}\frac{I_b}{V_i} R_L = -A_{ie}\frac{1}{Z_{ie}} R_L \end{aligned}$$

Substituting the value of Z_{ie} from above,

$$A_{ve} = -\frac{A_{ie} R_L}{h_{ie} - h_{re} R_L A_{ie}} = -\frac{R_L}{\frac{h_{ie}}{A_{ie}} - h_{re} R_L}$$

Again substituting the value of A_{ie}, we get

$$A_{ve} = -\frac{R_L}{h_{ie}\frac{(1+h_{oe}R_L)}{h_{fe}} - h_{re}R_L}$$
$$= -\frac{h_{fe}R_L}{h_{ie}(1+h_{oe}R_L) - h_{fe}h_{re}R_L}$$
$$A_{ve} = -\frac{h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{fe}h_{re})R_L}$$

Let $h_{ie}h_{oe} - h_{fe}h_{re} = \Delta h$

Therefore,

$$A_{ve} = -\frac{h_{fe}R_L}{h_{ie} + \Delta h R_L} \tag{25}$$

(d) Output Impedence (Z_{oe})

The output impedence of the amplifier is the ratio of output voltage to the output current with input source V_S reduced to zero and replaced by its internal resistance R_S. The output current is assumed to be drawn from a voltage source V_o which is connected across the output terminals. Then the circuit is modified as shown in Fig. 9.

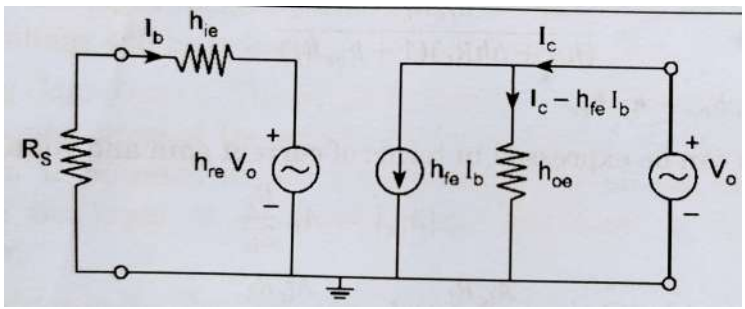

Figure 9: Circuit for determination of output impedence

From the output circuit of Fig.9, we get

$$I_c = h_{fe}I_b + h_{oe}V_o \tag{26}$$

From the input circuit,

$$I_b(R_S + h_{ie}) + h_{re}V_o = 0 \tag{27}$$

$$I_b = -\frac{h_{re}V_o}{h_{ie}+R_S}$$

Substituting the value of I_b in Eq.26, we get

$$\begin{aligned} I_c &= -h_{fe}\frac{h_{re}V_o}{h_{ie}+R_S} + h_{oe}V_o \\ &= \left(h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}+R_S}\right)V_o \\ &= \left(\frac{h_{oe}(h_{ie}+R_S) - h_{fe}h_{re}}{h_{ie}+R_S}\right)V_o \end{aligned}$$

Therefore the output impedence is,

$$Z_{oe} = \frac{V_o}{I_c} = \frac{h_{ie}+R_S}{h_{oe}(h_{ie}+R_S) - h_{fe}h_{re}} \tag{28}$$

Thus, the output impedence of the amplifier depends on the internal resistance of the source (R_S).

(e) Power Gain (A_{pe})

The power gain (A_{pe}) is defined as the ratio of the output ac power to the input ac power. Thus power gain is

$$A_{pe} = \frac{V_oI_o}{V_iI_i} = \left(\frac{V_o}{V_i}\right)\left(\frac{I_o}{I_i}\right) = |A_{ve}|\ |A_{ie}| \tag{29}$$

Substituting the values of A_{ve} and A_{ie}, we get

$$A_{pe} = \left(\frac{h_{fe}R_L}{h_{ie}+\Delta hR_L}\right)\left(\frac{h_{fe}}{1+h_{oe}R_L}\right)$$

$$A_{pe} = \left(\frac{h_{fe}^2R_L}{(h_{ie}+\Delta hR_L)(1+h_{oe}R_L)}\right) \tag{30}$$

where, $\Delta h = h_{ie}h_{oe} - h_{fe}h_{re}$

The power gain can be expressed in terms of current gain and voltage gain as follows: Since, $|A_{ve}| = A_{ie}\,{}_{\overline{R}\,L}Z_{ie}$

Therefore

$$A_{pe} = |A_{ve}|\ |A_{ie}| = \frac{A_{ie}R_L}{Z_{ie}} \times A_{ie} = \frac{A_{ie}^2R_L}{Z_{ie}}$$

$$A_{pe} = |A_{ve}|\ |A_{ie}| = A_{ie} \times \frac{A_{ve}Z_{ie}}{R_L} = \frac{A_{ve}^2Z_{ie}}{R_L}$$

6 Practical circuit for Common Emitter Transistor Amplifier

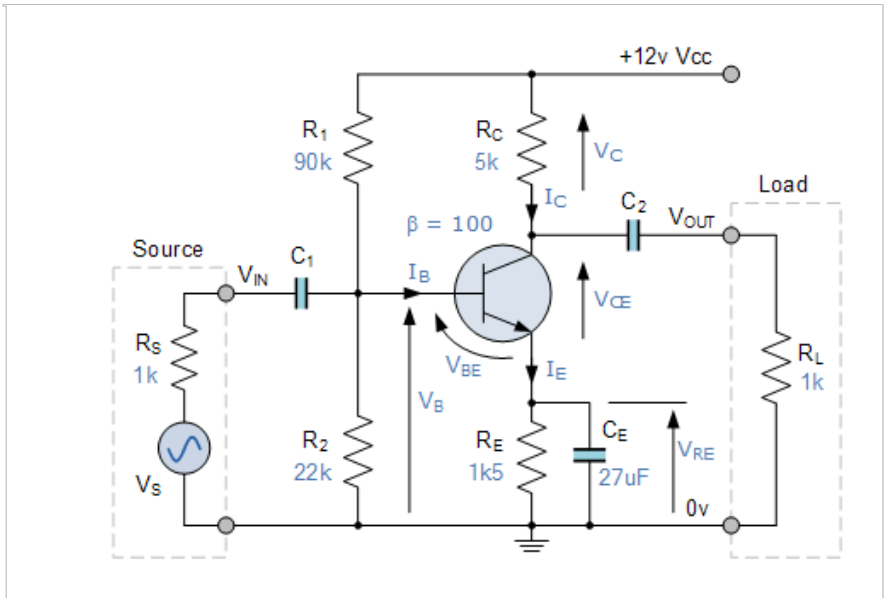

Figure 10: Single stage CE transistor amplifier

A practical single stage common emitter transistor amplifier is shown in Fig. 10. The various circuit elements and their functions are described below:

i. **Biasing Circuit**: Proper biasing and stabilisation is done by using voltage divider biasing method for which the resistors R_1, R_2 and R_E are used. It establishes a proper operating point in the middle of the load line.

ii. **Input Capacitor** C_1: The input capacitor is used to couple the input ac signal voltage to the base of the transistor. It allows only the ac signal from the input source to flow into the input circuit but isolates the signal source from R_2.

iii. **Emitter bypass capacitor** C_E: The capacitor C_E is connected across the emitter resistor R_E. It provides low reactance path to the alternating components of emitter current and works as a bypass capacitor.

iv. **Coupling Capacitor (C_2)**: The coupling capacitor is used to couple the output signal from the one stage of the amplifier to the load of the next stage of amplifier. It prevents the dc components of the output of the first stage from reaching the input of the second stage.

v. **Load resistance (R_L)**: The load resistance is the resistance of whatever is connected at the output. In case of multistage amplifier, the load resistance is the input resistance of the next stage.